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App. No.	:	10/756840
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For	:	SiGe STRAIN RELAXED BUFFER FOR HIGH MOBILITY DEVICES AND A METHOD OF FABRICATING IT

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TRANSMITTAL LETTER

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The attached documents are exact copies of the European patent application described on the following page, as originally filed.

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Patentanmeldung Nr. **Patent application No.** **Demande de brevet n°**

03447007.0

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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R C van Dijk

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

SiGe strain relaxed buffer for high mobility devices and a method of fabricating it

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SiGe STRAIN RELAXED BUFFER FOR HIGH MOBILITY DEVICES AND A METHOD OF FABRICATING IT

Field of the invention

[0001] The present invention is related to an epitaxial multilayer buffer suitable for the creation of high mobility devices on top of a semiconductor substrate. The present invention is further also related to a method to fabricate such a buffer.

State of the art

[0002] For years, digital electronics has been dominated by Si/SiO_2 based technology, because of the low cost of silicon and the properties (structural and electronic) of the Si/SiO_2 system. Since new applications are focused on wireless and optical communication, conventional silicon based devices do not offer anymore sufficient high frequency and opto-electronic properties. Nowadays, two materials/systems have the functionality required for these new applications: III-V materials (InP, GaAs,...) and IV-IV heterostructures (SiGe/Si).

[0003] Till now high frequency and optical applications mostly have been outclassed by the III-V materials grown on GaAs wafer, but the lack of natural oxide such as SiO_2 and the low level of integration possible on these wafers are major drawbacks.

[0004] SiGe/Si heterostructures comprising a strain adjusted SiGe layer and a strained Silicon layer improve

the electron transport into the strained silicon channel, thanks to a band offset at the heterointerface between SiGe and Si, which leads to the confinement of the electrons in a quantum well. The modification of the band structure is due to the lattice mismatch between Si and SiGe.

[0005] In order to benefit from both the functionality of these new systems and the advantages of silicon technology (low cost, high throughput and capacities), one solution is to integrate III-V compounds or SiGe/Si on Si substrate. The main challenge is then to deposit these materials on a substrate, which has a different lattice parameter. The lattice mismatch between the film and the substrate gives rise to the formation and the propagation of dislocations into the epilayer. Each dislocation in the active part of the epitaxial layer leads to the deterioration of the electronic properties and of the carrier transport due to scattering.

[0006] The density of dislocations rising to the top of the epitaxial layer can be as high as 1E11 cm^{-2} for SiGe and 1E10 cm^{-2} for GaAs, which is too high for any application. In order to grow high functionality materials it is necessary to keep the dislocation density in the active part of the epitaxial layer as low as possible and preferably below 1E4 cm^{-2}, although this specification is not well established yet.

[0007] One solution to grow SiGe and III-V compounds on top of Si substrate without any defects is to insert a Strain Relaxed SiGe Buffer (SRB) between substrate and hetero-system. The characteristics of SiGe make it a suitable compound for SRB application. Furthermore it is possible on Si substrates to adapt SiGe layer systems with 0 (pure Si) to 4,16% (100% Ge) lattice mismatch, determined by the Ge content in the SRB.

[0008] Although rather high electron mobility and low threading dislocation density can be obtained, thick graded buffers still present some major economical and technological drawbacks: growth time, material consumption, too large step height for integration with Si microelectronics. To overcome these problems, many efforts have been carried out on Thin Strain Relaxed Buffer (TSRB).

[0009] An epitaxial layer can only relax over a critical thickness by introducing dislocations into the epitaxial layer. This critical thickness is mainly determined by the growth conditions (growth rate, temperature,...) and by the defects present in the epilayer and/or at the heterointerface. The TSRB employs defects in order to reduce this critical thickness and to confine the dislocations at the heterointerface.

[0010] There are three main methods to do this, namely in situ defect creation, ex situ defect creation and compliant substrate. In the invention the in-situ method is used, in which grown-in point defects can act as nucleation sites for misfit dislocations and significantly reduce the critical thickness. The principle of this method is to grow the defects during the deposition of the SRB.

[0011] Several researchers have been working on this type of SRB, by using Molecular Beam Epitaxy (MBE), Ultra High Vacuum Chemical Vapor Deposition (UHV-CVD) or Low-Energy Plasma Enhanced Chemical Vapor Deposition (LEPECVD). These methods lead to a high degree of relaxation for the top layer (>90%) for very low thickness (200 nm), while the dislocations are confined into the low temperature epilayer.

[0012] The main drawback of these methods is that they are only applicable for MBE, UHV-CVD or LEPECVD systems. As in RPCVD systems, the growth rate is strongly

linked to the growth temperature; the growth at ultra low temperature would be very slow or even impossible.

[0013] A patent related to the present invention is Patent WO 01/73827 by Matsushita. It describes how an annealed SiGeC crystal layer, comprising a matrix SiGeC crystal layer relaxed in lattice and almost free from dislocations and SiC microcrystals dispersed in the layer, is formed on an Si substrate by heat-annealing an SiGeC crystal layer-deposited Si substrate. Then, a Si crystal layer is deposited on an annealed SiGeC crystal layer to form a distorted Si crystal layer with a minimum dislocation. The main differences with the solution presented by the invention lie in the different principle of threading dislocation reduction used and in the degree of relaxation reached.

Aims of the invention

[0014] The present invention aims to disclose a SiGe strain relaxed buffer (TSRB) with improved features for high mobility devices and to provide a simple, reliable method to grow a TSRB on a semiconductor substrate.

Summary of the invention

[0015] The invention relates to a semiconductor device comprising a semiconductor substrate and on top of that a Thin Strain Relaxed Buffer, consisting of three layers. All three layers of said Thin Strain Relaxed Buffer have a same, constant Ge concentration. The three layers are :

- a first epitaxial layer of $Si_{1-x}Ge_x$, x being the Ge concentration,

- a second epitaxial layer of $Si_{1-x}Ge_x$: C on said first epitaxial layer, the amount of C being at least 0.3 %, and
- a third epitaxial layer of $Si_{1-x}Ge_x$ on said second layer.

[0016] In a preferred embodiment of the semiconductor device the thickness of said second epitaxial layer is between 1 and 20 nm.

[0017] In an even more specific embodiment the thickness of said second epitaxial layer is between 1 and 10 nm.

[0018] In an ideal embodiment the thickness of said second epitaxial layer is 5 nm.

[0019] Advantageously the Ge concentration is between 5 and 100 %.

[0020] In a more specific embodiment the Ge concentration is between 10 and 65 %.

[0021] In another preferred embodiment the semiconductor device further has a SiGe/Si heterostructure at the top of the TSRB. The heterostructure comprises a strain adjusted SiGe layer and a strained Silicon layer.

[0022] In an alternative preferred embodiment the Thin Strain Relaxed Buffer has a III-V compound at its top.

[0023] As a second object the present invention relates to a method to grow a Thin Strain Relaxed Buffer, comprising the steps of:

- Providing a semiconductor substrate,
- Depositing a first epitaxial layer SiGe on top of said semiconducting substrate in such a way that the Ge concentration is essentially constant throughout said first layer,
- Depositing a second layer SiGe:C, on top of said first SiGe epitaxial layer, by growing SiGe incorporating at least 0.3 % carbon, and in such a way that the Ge

concentration is essentially constant throughout said SiGe:C layer and the same as in said first layer,

- Depositing a second SiGe epitaxial layer on top of said SiGe:C layer, in such a way that the Ge concentration is essentially constant throughout said third layer.

[0024] Advantageously, the semiconductor substrate is silicon.

[0025] Preferably the Ge concentration is between 5 and 100%, and even more advantageously it is between 10 and 65%.

[0026] According to a specific embodiment, a first and a second precursor gas are provided. The first precursor gas is a Si containing compound or a compound from the SiH_zCl_w group with z and w equal to 1-4, and the second precursor gas is a Ge bearing precursor compound. The layers are deposited making use of said precursor gases.

[0027] According to another specific embodiment a carbon containing gas is provided, being any C bearing compound.

[0028] In another embodiment the method contains an additional step, in which the structure consisting of said semiconductor substrate and said three epitaxial layers is exposed to a temperature of 800°C or higher, whereby the maximum temperature is defined by the melting point of said SiGe layer.

[0029] In a preferable embodiment the method comprises the additional step of depositing a strain adjusted SiGe layer on top of a Thin Strain Relaxed Buffer.

[0030] Advantageously the method comprises the additional step of depositing a strained silicon layer on top of said strain adjusted SiGe layer.

[0031] In a specific embodiment said substrate is a blanket wafer.

[0032] In an alternative embodiment said substrate is a patterned wafer.

Short description of the drawings

[0033] Fig. 1 represents a scheme of the system, containing the TSRB SiGe epitaxial layer.

[0034] Fig. 2 represents the TSRB structure in case of selective growth.

Detailed description of the invention

[0035] The invention relates to a Thin Strain Relaxed Buffer (TSRB) for the integration of high mobility devices (for example SiGe/strained Si system) on top of a semiconductor substrate like e.g. Silicon. In the following description both the Thin Strain Relaxed Buffer and the method to obtain it are explained.

[0036] One grows epitaxially a TSRB based on $Si_{0.78}Ge_{0.22}$ / $Si_{0.78}Ge_{0.22}$: C_y / $Si_{0.78}Ge_{0.22}$ multilayer system, with y (C concentration) at least 0.3%. 91 % relaxation was reached after rapid thermal annealing (30″ at 1000°C) of the TSRB, with a very smooth surface (RMS~1nm). No dislocations are observed reaching the surface of the epitaxial layer. Carbon is incorporated during the growth of SiGe with the in-situ method, in order to create heterogeneous centres for dislocation nucleation.

[0037] In figure 1 is represented a complete structure of a 230 nm TSRB according to the invention on a silicon substrate with a SiGe/Si hetero-system deposited at its top. Although the TSRB is suitable for the adjustment at its top of both a SiGe/Si heterostucture and III-V compounds, the focus in this description is on the SiGe/Si integration on the TSRB.

[0038] Before growing the Thin Strain Relaxed Buffer a native oxide layer is removed from the substrate. The

TSRB in Fig.1 consists of a first epitaxial layer $Si_{0.78}Ge_{0.22}$, a second epitaxial layer $Si_{0.78}Ge_{0.22}:C_y$ and a third epitaxial layer $Si_{0.78}Ge_{0.22}$. The thickness of said second $Si_{0.78}Ge_{0.22}$ layer is between 1 and 20 nm, 5 nm being an ideal value. In all three layers the Ge concentration has an essentially constant value : a constant Ge concentration should be understood as also allowing small deviations from said constant value in the Ge profile. In the example of Fig.1 a Ge concentration of 22 % is used. The Ge concentration can in principle have any value in the range from 5 to 100%, assuming the growth conditions are such that 3-dimensional grow can be avoided. However, the higher the Ge concentration the more difficult to keep advantageous growth conditions.

[0039] For the epitaxial deposition of the TSRB several methods can be envisaged. One can use e.g. an Epsilon-One Atmospheric Pressure/Reduced Pressure Chemical Vapor Deposition (AP/RPCVD) epitaxial reactor. This is a single wafer (allowed wafer size: 4″ to 12″), horizontal and load locked reactor, with a lamp heated graphite susceptor in a rectangular quartz tube. A first precursor gas, containing Si, and a second precursor gas containing Ge, can be used for the deposition of the epitaxial layers. Further a carrier gas (e.g. H_2) can possibly be employed. The first precursor gas can in fact be any Si containing compound, such as, but not limited to, silane, disilane or higher silanes, or any compound from the SiH_zCl_w group with z and w equal to 1-4. The second precursor gas can be any Ge bearing precursor compound such as but not limited to GeH_4, $GeCl_4$ or any other Ge containing compound. The following procedure can be used for the growth of the TSRB:

- Loading of the wafer from the load lock to the growth chamber,

- Removing any native silicon oxide or traces of oxide by any means such as dissolution of the oxide in aqueous HF solutions, if needed followed by in-situ baking in an epitaxy tool according to a standard procedure,
- Deposition of the epitaxial layers at about 600°C for SiGe and SiGe:C, and at about 650°C for Si,

In order to add the carbon, a carbon containing gas can be provided. This can be any C bearing compound such as, but not limited to, $SiH_z(CH_3)_w$ with z and w equal to 1-4. At least 0.3 % carbon is to be incorporated, ideally between 0.3 and 1 %.

[0040] The TSRB can be grown by AP/RP CVD as explained in this text, but any other means of depositing epitaxial Si containing layers are suitable, such as e.g. Molecular Beam Epitaxy, Low Pressure CVD (LPCVD), plasma enhanced CVD, optically enhanced CVD, and so on, as long as they are able to deposit layer structures as specified in the invention.

[0041] In a following step the TSRB is exposed to a high temperature in the range from 800°C up to the melting temperature, which depends on the Ge concentration. For pure Si the melting temperature is 1410°C and for $Si_{1-x}Ge_x$ 937°C for pure Ge. A method like e.g. a rapid thermal annealing procedure can be applied. For the rapid thermal annealing of the TSRB a 50°C/sec ramped temperature profile is chosen with an intermediate step of 5s at 700°C. The samples are annealed for 30 seconds at 1000°C, with Nitrogen as carrier gas. The samples are cooled down for 20 minutes into the furnace in order to avoid oxidation of the surface of the sample.

[0042] For the deposition of the strain adjusted $Si_{1-x}Ge_x$ layer on the TSRB, the TSRB is first cleaned, followed by a 30″ etching procedure into HF(2%). The TSRB

then is placed into the epsilon load lock for 1 hour of nitrogen purge. Before deposition, there is a 3 minute bake at 850°C. Other procedures can be followed to obtain the same result.

[0043] The surface of the layers is checked by means of a Nomarsky interference microscope. Ellipsometric spectroscopy is used to determine the Ge content and the thickness of the layers, by using ASET-F5 tool (Advanced Spectroscopic Ellipsometry Technology) from KLA-TENCOR. The IR absorption spectra is measured by a Fourier Transform Infra Red absorption tool. The surface Root Mean Square roughness is checked by AFM (tapping mode). In order to avoid excessive long time of measurements, a light scattering tool (SP1/KLA TENCOR) is used to measure the low frequency component of the output signal.

[0044] In the previous, blanket wafers were considered, i.e. without patterns at the surface of the silicon wafers. The described method can however be modified for the growth of TSRB on patterned wafers. Latter wafers present both silicon and Shallow Trench Insulator (STI) trenches filled with SiO_2. These STI structures are used as electrical insulators between the transistors. Fig.2 shows the final structure of the selective TSRB. Also other isolation structures such as LOCOS or others can be present.

[0045] The aim of the selective epitaxial deposition of the TSRB is to avoid any problems due to the formation of STI trenches into the $Si_{1-x}Ge_x$ buffer (and Strained silicon). Because of the thermal instability of strained silicon, and the chemical reactivity of SiGe, which is different from silicon, this module contains some critical steps, such as the oxidation of SiGe/Si and resist strip after trench formation. Thanks to the selective growth of the TSRB and the Strained Silicon, the STI module keeps

standard steps and therefore the integration of the TSRB/Strained Si system becomes much easier than in case of a conventional non-selective growth.

[0046] The system used for the deposition is the same as the one used for the non-selective growth.

The process is the following:

a) removing any native silicon oxide or traces of oxide by any means such as dissolution of the oxide in aqueous HF solutions, if needed followed by in-situ baking in an epitaxy tool according to a standard procedure

b) The TSRB is then grown at 650°C using DichloroSilane (DCS), Germane en MonoMethylSilane (MMS) as precursor gases. By using HCl during the deposition it is then possible to grow selectively (i.e. only on the silicon) the TSRB. Also other Si, C and Ge precursor gases could be used as long as the deposition remains selective.

[0047] So, it is possible to deposit selectively the TSRB on a patterned wafer (with oxide structures) with the same characteristics: high relaxation, smooth and no threading dislocations reaching the surface of the TSRB.

[0048] By using the selective growth of TSRB, the TSRB+Strained Silicon is deposited after the STI formation and therefore the STI module is kept unchanged (standard CMOS). The integration of the TSRB into standard CMOS process flow is therefore much easier. One can therefore skip the critical steps in the STI module which are the oxidation of TSRB/ Strained Si and the resist strip after the etching of the STI trenches.

CLAIMS

1. A semiconductor device comprising a semiconductor substrate and having on its top at least a Thin Strain Relaxed Buffer, consisting of three layers, **characterised in that** all three layers of said Thin Strain Relaxed Buffer have an essentially constant Ge concentration, said three layers being :

- a first epitaxial layer of $Si_{1-x}Ge_x$, x being the Ge concentration
- a second epitaxial layer of $Si_{1-x}Ge_x$: C on said first epitaxial layer, the amount of C being at least 0.3 %
- a third epitaxial layer of $Si_{1-x}Ge_x$ on said second layer.

2. A semiconductor device, as in claim 1, **characterised in that** the thickness of said second epitaxial layer is between 1 and 20 nm.

3. A semiconductor device, as in claim 1, **characterised in that** the thickness of said second epitaxial layer is between 1 and 10 nm.

4. A semiconductor device, as in claim 1, **characterised in that** the thickness of said second epitaxial layer is 5 nm.

5. A semiconductor device, as in claim 1, **characterised in that** the Ge concentration is between 5 and 100 %.

6. A semiconductor device as in claim 1, **characterised in that** the Ge concentration is between 10 and 65 %.

7. The semiconductor device, as in any of the claims 1 to 6, **characterised in that** it has further a SiGe/Si heterostructure at the top of the Thin Strain Relaxed Buffer, said heterostructure comprising a strain adjusted SiGe layer and a strained Silicon layer.

8. The semiconductor device, as in any of the claims 1 to 6, **characterised in that** it has a III-V compound at its top.

9. A method to grow a Thin Strain Relaxed Buffer, comprising the steps of

- Providing a semiconductor substrate,
- Depositing a first epitaxial layer SiGe on top of said semiconducting substrate in such a way that the Ge concentration is essentially constant throughout said first layer,
- Depositing a second layer SiGe:C, on top of said first SiGe epitaxial layer, by growing SiGe incorporating at least 0.3 % carbon, and in such a way that the Ge concentration is essentially constant throughout said SiGe:C layer and the same as in said first layer,
- Depositing a second SiGe epitaxial layer on top of said SiGe:C layer, in such a way that the Ge concentration is essentially constant throughout said third layer.

10. The method according to claim 9, **characterised in that** said semiconductor substrate is silicon.

11. The method according to claim 9, **characterised in that** said Ge concentration is between 5 and 100%.

12. The method according to claim 9, **characterised in that** said Ge concentration is between 10 and 65%.

13. The method according to claim 9, whereby a first and a second precursor gas are provided **characterised in that** said first precursor gas is a Si containing compound or a compound from the SiH_zCl_w group with z and w equal to 1-4, and said second precursor gas is

a Ge bearing precursor compound **and in that** said layers are deposited making use of said precursor gases.

14. The method according to claim 9, **characterised in that** a carbon containing gas is provided, being any C bearing compound.

15. The method according to claim 9, **characterised in that** in an additional step the structure consisting of said semiconductor substrate and said three epitaxial layers is exposed to a temperature of 800°C or higher, whereby the maximum temperature is defined by the melting point of said SiGe layer.

16. The method according to any of the claims 9 to 15, comprising the additional step of depositing a strain adjusted SiGe layer on top of a Thin Strain Relaxed Buffer.

17. The method according to claim 16, comprising the additional step of depositing a strained silicon layer on top of said strain adjusted SiGe layer.

18. The method according to claim 9, **characterised in that** said substrate is a blanket wafer.

19. The method according to claim 9, **characterised in that** said substrate is a patterned wafer.

ABSTRACT

SiGe STRAIN RELAXED BUFFER FOR HIGH MOBILITY DEVICES AND A METHOD OF FABRICATING IT

The invention relates to a semiconductor device comprising a semiconductor substrate and having on its top at least a Thin Strain Relaxed Buffer, consisting of three layers, **characterised in that** all three layers of said Thin Strain Relaxed Buffer have an essentially constant Ge concentration, said three layers being :

- a first epitaxial layer of $Si_{1-x}Ge_x$, x being the Ge concentration
- a second epitaxial layer of $Si_{1-x}Ge_x$: C on said first epitaxial layer, the amount of C being at least 0.3 %
- a third epitaxial layer of $Si_{1-x}Ge_x$ on said second layer.

(Figure 1)

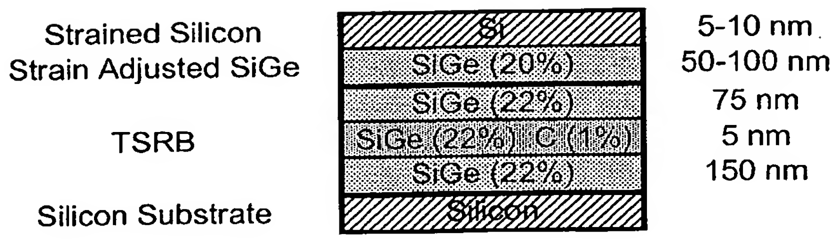
Strained Silicon
Strain Adjusted SiGe
TSRB
Silicon Substrate
Si
SiGe (20%)
SiGe (22%)
SiGe (22%) C (1%)
SiGe (22%)
Silicon
5-10 nm
50-100 nm
75 nm
5 nm
150 nm

Fig. 1

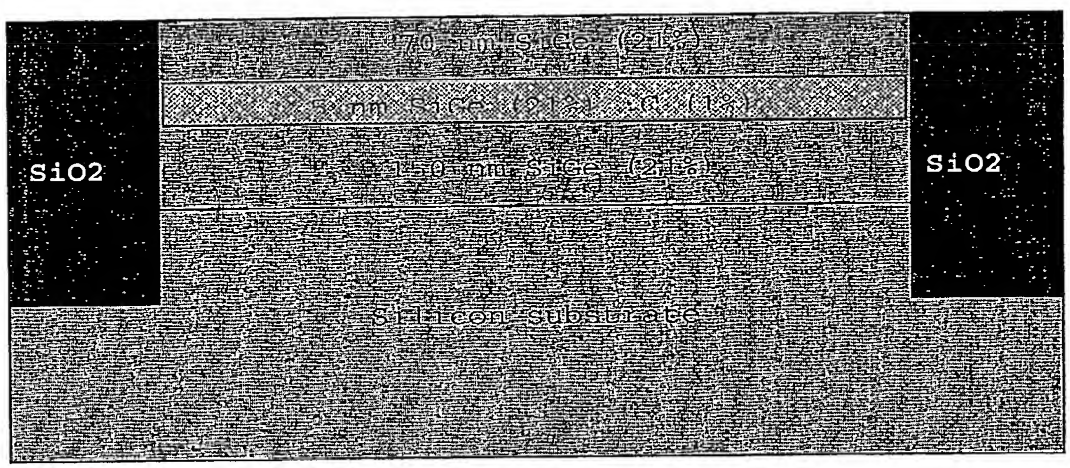
70 nm SiGe (21%)
5 nm SiGe (21%) C (1%)
150 nm SiGe (21%)
SiO2
SiO2
Silicon substrate

Fig. 2